REMARKS

Drawings. In the Non-Final Office Action, Examiner Shapiro objected to the drawings as failing to show each limitation of independent claim 9. The Applicant respectfully traverses this objection, because each limitation of claim 9 is illustrated in the drawings. Specifically, the following recites support for each limitation of claim 9 in FIGS. 1-5:

1. First limitation of independent claim 9: "a substrate" is the substrate 25 shown in FIGS. 1, and 3-5;

2. Second limitation of independent claim 9: "an array of individually addressable matrix elements carried on said substrate" is the array of individually addressable matrix elements 10 carried on substrate 25 as shown in FIG. 1;

3. Third limitation of independent claim 9: "a set of address conductors connected to said array of matrix elements and carried on said substrate" is the a set of address conductors 16 connected to elements 10 and carried on substrate 25 as shown in FIGS. 1-5;

4. Fourth limitation of independent claim 9: "said set of address conductors being arranged in a series of groups with each group including successive address conductors" is the arrangement in a series of groups with each group including successive address conductors with the first group being address conductors C1-C9 which are collectively controlled by a gate signal G1 via control circuit 37 as shown in FIG. 2, the second group being address conductors C10-C18 which are collectively controlled by a gate signal G2 via control circuit 37 as shown in FIG. 2, and so on and so on;

5. Fifth limitation of independent claim 9: "an addressing circuit" is the addressing circuit 35 shown in FIGS. 1-5;

6. Sixth limitation of independent claim 9: "a multiplexing circuit integrated on said substrate and connected to said set of address conductors" is the multiplexing circuit 31 integrated on substrate 25 and connected to address conductors 16 as illustrated in FIGS. 3-5;

7. Seventh limitation of independent claim 9: "said multiplexing circuit including a plurality of signal bus lines" are the signal bus lines V1-V9 shown in FIGS. 3-5.

8. Eight limitation of independent claim 9: "said multiplexing circuit being arranged to couple sequentially each group of said set of address conductors to said plurality of signal bus lines with each address conductor in a group being coupled to a respective one of said signal bus lines" is the arrangement as shown in FIG. 2 of the first address conductor of each group (e.g., conductors C1 and C10) being connected to signal bus line V1, the second address conductor of each group (e.g., conductors C2 and C11) being connected to signal bus line V2, the third address conductor of each group (e.g., conductors C3 and C12) is connected to signal bus line V3, the fourth address conductor of each group (e.g., conductors C4 and C13) being connected to signal bus line V4, the fifth address conductor of each group (e.g., conductors C5 and C14) being connected to signal bus line V5, the sixth address conductor of each group (e.g., conductors C6 and C15) being connected to signal bus line V6, the seventh address conductor of each group (e.g., conductors C7 and C16) being connected to signal bus line V7, the eighth address conductor of each group (e.g., conductors C8 and C17) being connected to signal bus line V8, and the ninth address conductor of each group (e.g., conductors C9 and C18) being connected to signal bus line V9.

9. Ninth limitation of independent claim 9: "a plurality of signal processing circuits integrated on said substrate" are the signal processing circuits 42(1)-42(9) integrated on substrate 25 as shown in FIGS. 3-5;

10. Tenth limitation of independent claim 9: "each signal processing circuit being connected to a respective bus line" is the signal processing circuit 42(1) being connected to bus line V1 as shown in FIGS. 3-5, the signal processing circuit 42(2) being connected to bus line V2 as shown in FIGS. 3-5, the signal processing circuit 42(3) being connected to bus line V3 as shown in FIGS. 3-5, the signal processing circuit 42(4) being connected to bus line V4 as shown in FIGS. 3-5, the signal processing circuit 42(5) being connected to bus line V5 as shown in FIGS. 3-5, the signal processing circuit 42(6) being connected to bus line V6 as shown in FIGS. 3-5, the signal processing circuit 42(7) being connected to bus line V7 as shown in FIGS. 3-5, the signal processing circuit 42(8) being connected to bus line V8 as shown in FIGS. 3-5 and the signal processing circuit 42(9) being connected to bus line V9 as shown in FIGS. 3-5; and

11. Eleventh limitation of independent claim 9: "wherein a first signal processing circuit associated with a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate" is the signal processing circuit 42(1) associated with a first address conductor C10 of a first group of address conductors C10-C18 and a second signal processing circuit 42(9) associated with a last address conductor C9 of a second group of address conductors C1-C9 are adjacent on said substrate 25 as shown in FIGS. 4 and 5. This should be compared to the prior art shown in FIG. 3 where signal processing circuits 42(1) and 42(9) are not adjacent on substrate 25.

Withdrawal of the objection of the drawings as failing to show each limitation of independent claim 9 is therefore respectfully requested.

Specification. In the Non-Final Office Action, Examiner Shapiro objected to the specification as failing to provide an antecedent basis for independent claim 9. The Applicant respectfully traverses this objection, because the specification clearly provides an antecedent basis for each limitation of claim 9. See, *U.S. Patent Application Serial No. 09/614,154* at page 6, line 5 to page 12, line 19. In particular, signal processing circuits 42(1) and 42(9) being adjacent on the substrate is taught at page 11, line 23 to page 12, line 13.

Withdrawal of the objection of the specification as failing to provide an antecedent basis for independent claim 9 is therefore respectfully requested.

Claims. In the Non-Final Office Action, Examiner Shapiro rejected pending claims 9, 10, 12 and 13 on various grounds. The Applicant responds to each rejection as subsequently recited herein, and respectfully requests reconsideration of the present application:

A. Examiner Shapiro rejected pending claim 9 under 35 U.S.C. §112, ¶2 as being indefinite

The Applicant has thoroughly considered Examiner Shapiro's remarks concerning the claim 9 as being indefinite. The Applicant respectfully traverses this indefinite, because it is clear how the main objective of the present invention is achieved as shown in FIGS. 4 and 5 with the physical order of signal processing circuits 42(1)-42(9) being different than the prior art physical order shown in FIG. 3. Specifically, signal processing circuits 42(1) and 42(9) are adjacent on substrate 25 as shown in FIGS. 4 and 5, and signal processing circuits 42(1) and 42(9) are far apart on substrate 25 as shown in FIG. 3. Please note the teachings on page 4, lines 3-23 of the present application are directed to the drawbacks of FIG. 3, and the teachings on page 4, lines 23-28 are directed to overcoming the drawbacks of FIG. 3 as exemplary shown in FIGS. 4 and 5.

Withdrawal of the rejection of independent claim 9 under 35 U.S.C. §112, ¶2 as being indefinite is therefore respectfully requested.

B. Examiner Shapiro rejected pending claims 9 and 10 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,166,715 to *Chang* et al. in view of U.S. Patent No. 5,021,774 to *Ohwada* et al.

The Applicant has thoroughly considered Examiner Shapiro's remarks concerning the patentability of claims 9 and 10 over *Chang* in view of *Ohwada*. The Applicant has also thoroughly read *Chang* and *Ohwada*. To warrant this 35 U.S.C. §103(a) rejection of claims 9 and 10, all the claim limitations recited in independent claim 9 must be taught or suggested by the combination of *Chang* and *Ohwada*. See, MPEP §2143. The Applicant respectfully traverses this §103(a) rejection of claims 9 and 10, because neither *Chang* nor *Ohwada* disclose, teach or suggest "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein a first signal processing circuit associated with a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate" as recited in independent claim 9.

As to the traversal, Examiner Shapiro has correctly recognized *Chang*'s failure to teach or suggest the last limitation of independent claim 9. Specifically, as illustrated in FIGS. 3 and 4, *Chang* teaches signal processing circuit 245_1 to 245_{40} where signal processing circuit 245_1 is associated with the first address conductors PIX1, PIX41, PIX81, PIX121, PIX161, PIX201, PIX241, PIX281, PIX321, PIX361, PIX401, PIX441, PIX481, PIX521, PIX561 and PIX601 of groups 1-16, respectively, and where signal processing circuit 245_{40} is associated with the last address conductors PIX40, PIX80, PIX120, PIX160, PIX200, PIX240, PIX280, PIX320, PIX360, PIX400, PIX440, PIX480, PIX520, PIX560, PIX600 and PIX640 of groups 1-16, respectively. *Chang*'s fails to teach or suggest the last limitation of independent claim 9 by teaching signal processing circuit 245_1 and signal processing circuit 245_{40} are not adjacent as shown in FIG. 3.

Thus, *Ohwada* must teach or suggest the last limitation of independent claim 9 in order to establish a prima facie case of obviousness. However, Examiner Shapiro has erroneously interpreted *Ohwada* as teaching the last limitation of independent claim 9, because a proper reading of *Ohwada* reveals that *Ohwada* also fails to teach or suggest the last limitation of independent claim 9.

Specifically, the last limitation of independent claim 9 is each individual signal processing circuit being associated with a first address conductor of a first group and a last address conductor of a second group are adjacent on the substrate. This limitation is neither taught nor suggested by *Ohwada* by the disclosure of a multiplexor, a single group of address conductors and a single signal processing circuit. Specifically, as shown in FIGS. 1, 2 and 7, the multiplexor of *Ohwada* consists of a voltage generator 3, TFT elements 2, sampling lines 5, and sampling TFT elements 6 that operate to sample and hold video input signal V_V on capacitors 7 in a sequential manner during a beginning portion of a scanning period via signals ø and CP. During a final portion of the scanning period, all capacitors 7 are simultaneously discharged as a single group by the single group of address conductors via a voltage V_{SS}, where each address conductor consists of a TFT element 10, a buffer 11 and a signal electrode 12. As illustrated in FIG. 4, the video input signal V_V is a single signal coming from a single processing circuit. *Ohwada* clearly does not teach groups of address conductors and a plurality of signal processing circuits, and thus fails to teach or suggest the last limitation of independent claim 9.

In summary, the last limitation of independent claim 9 is directed to FIGS. 4 and 5 of the present application, and therefore the combination of *Chang* in view of *Ohwada* unequivocally fails to teach the last limitation of independent claim 9. Additionally, *Chang* teaches away from the last limitation of independent claim 9 by teaching a sequential control by a shift register 230 of the switches A1, A2, B1 and B2 of each signal processing circuit 245_1 to 245_{40} that is simplified based on the sequential arrangement of signal processing circuit 245_1 to 245_{40} as shown in FIG. 3.

Withdrawal of the rejection of independent claim 9 under 35 U.S.C. §103(a) as being unpatentable over *Chang* in view of *Ohwada* is therefore respectfully requested.

Claim 10 depends from independent claim 9. Therefore, dependent claim 10 includes all of the elements and limitations of independent claim 9. It is therefore respectfully

submitted by the Applicant that dependent claim 10 is allowable over *Chang* in view of *Ohwada* for at least the same reason as set forth herein with respect to independent claim 9 being allowable over *Chang* in view of *Ohwada*. Withdrawal of the rejection of dependent claim 10 under 35 U.S.C. §103(a) being unpatentable over *Chang* in view of *Ohwada* is therefore respectfully requested.

C. Examiner Shapiro rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,384,806 to *Chang* et al. in view of U.S. Patent No. 5,021,774 to *Ohwada* et al. and in further view of U.S. Patent No. 6,384,806 to *Matsueda* et al.

Claim 12 depends from independent claim 9. Therefore, dependent claim 12 includes all of the elements and limitations of independent claim 9. It is therefore respectfully submitted by the Applicant that dependent claim 12 is allowable over *Chang* in view of *Ohwada* and in further view of *Matsueda* for at least the same reason as set forth herein with respect to independent claim 9 being allowable over *Chang* in view of *Ohwada*. Withdrawal of the rejection of dependent claim 12 under 35 U.S.C. §103(a) being unpatentable over *Chang* in view of *Ohwada* and in further view of *Matsueda* is therefore respectfully requested.

D. Examiner Shapiro rejected claim 13 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,021,774 to *Ohwada* et al. in view of U.S. Patent No. 6,384,806 to *Matsueda* et al.

The Applicant has thoroughly considered Examiner Shapiro's remarks concerning the patentability of claim 13 over *Ohwada* in view of *Matsueda*. The Applicant has also thoroughly read *Ohwada* and *Matsueda*. To warrant this 35 U.S.C. §103(a) rejection of claim 13, all the claim limitations recited in independent claim 13 must be taught or suggested by the combination of *Ohwada* and *Matsueda*. See, MPEP §2143. The Applicant respectfully traverses this §103(a) rejection of claim 13, because neither *Ohwada* and *Matsueda* in combination fails to teach and *Ohwada* teaches away from the following limitations of independent claim 13:

1. "a set of address conductors connected to said array of matrix elements and carried on said substrate, said set of address conductors being arranged in a series of groups with each group including successive address conductors" as recited in independent claim 13;

2. "a multiplexing circuit integrated on said substrate and connected to said set of address conductors, said multiplexing circuit including a plurality of signal bus lines, said multiplexing circuit being arranged to couple sequentially each group of said set of address conductors to said plurality of signal bus lines with each address conductor in a group being coupled to a respective one of said signal bus lines" as recited in independent claim 13; and

3. "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein an order in which said signal processing circuits are arranged physically on said substrate is at least partially different than a physical order of said signal bus lines to which said signal processing circuit blocks are respectively connected" as recited in independent claim 13.

Specifically, the aforementioned limitations of independent claim 13 are neither taught nor suggested by *Ohwada* by the disclosure of a multiplexor, a single group of address conductors and a single signal processing circuit. Specifically, as shown in FIGS. 1, 2 and 7, the multiplexor of *Ohwada* consists of a voltage generator 3, TFT elements 2, sampling lines 5, and sampling TFT elements 6 that operate to sample and hold video input signal V_V on capacitors 7 in a sequential manner during a beginning portion of a scanning period via signals ø and CP. During a final portion of the scanning period, all capacitors 7 are simultaneously discharged as a single group by the single group of address conductors via a voltage V_{ST}, where each address conductor consists of a TFT element 10, a buffer 11 and a signal electrode 12. As illustrated in FIG. 4, the video input signal V_V is a single signal coming from a single processing circuit. *Ohwada* clearly does not teach groups of address

conductors and a plurality of signal processing circuits, and thus fails to teach or suggest the aforementioned limitations of independent claim 13. Moreover, *Ohwada* teaches away from the aforementioned limitations of independent claim 13, because any modification of *Ohwada* to encompass the aforementioned limitations of independent claim 13 would clearly change the principle operation of *Ohwada* as prohibited by the obviousness standard.

Thus, a teaching or suggest of the last limitation of independent claim 13 by *Matsueda* in order to establish a prima facie case of obviousness is immaterial in view of *Ohwada* teaching away from the aforementioned limitations of independent claim 13.

Nonetheless, the video bus lines V1-V9 (FIGS. 2-5) of the present invention are taught by *Matsueda* as a 6 bit signal bus line to multiplexing circuit 101 of *Matsueda* (FIG. 15), a 8 bit signal bus line to multiplexing circuit 101' of *Matsueda* (FIG. 16), and signal bus lines D1B-DuB and D1T-DuT to multiplexing circuits 101A and 101B, respectively, of *Matsueda* (FIG. 17). The teaching of the aforementioned bus lines arguably implies an existence of signal processing circuits for providing the 6 bit signal bus line to multiplexing circuit 101 of *Matsueda* (FIG. 15), an existence of signal processing circuits for providing the 8 bit signal bus line to multiplexing circuit 101' of *Matsueda* (FIG. 16), and an existence of signal processing circuits for providing signal bus lines D1B-DuB and D1T-DuT to multiplexing circuits 101A and 101B, respectively, of *Matsueda* (FIG. 17). However, if they exist, these implied signal processing circuits are not illustrated in FIGS. 15-17 of *Matsueda*, and more importantly, *Matsueda* fails to provide any teachings related to the physical order of these implied signal processing circuits on the substrates for supporting circuits 101, 101', 101A and 101B, respectively. This is particular evidenced by the failure of *Matsueda* to state any display quality problem related to the physical order of these implied signal processing circuits on the substrates for supporting circuits 101, 101', 101A and 101B, respectively.

Thus, at best, the physical order of these implied signal processing circuits on the substrates for supporting circuits 101, 101', 101A and 101B, respectively, must be deemed to be no more than cumulative to the prior art illustrated in FIG. 3 of the present invention.

Furthermore, Examiner Shapiro's assertion that column 20, lines 29-45 of *Matsueda* teaches the last limitation of independent claim 13 is erroneous, because that portion of

Matsueda is related to capacitive lines 43 in the context of scanning lines 42, which are unrelated to the last limitation of independent claim 13.

Withdrawal of the rejection of independent claim 13 under 35 U.S.C. §103(a) as being unpatentable over *Ohwada* in view of *Matsueda* is therefore respectfully requested.

SUMMARY

Examiner Shapiro's objections to the drawings and specification, and indefiniteness rejection of independent claim 9 have been obviated herein by remarks directed to showing support for each limitation of independent claim 9 in FIGS. 1-5. Examiner's Shapiro's rejections of claims 9, 10 and 12 have been obviated by the remarks herein supporting an allowance of pending claims 9, 10 and 12 over *Chang* in view of *Ohwada*. Examiner Shapiro's rejection of claim 13 has been obviated by the remarks herein supporting an allowance of pending claim 13 over *Ohwada* in view of *Matsueda*. The Applicant respectfully submits that claims 9-13 as listed herein fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, Examiner Shapiro is respectfully requested to contact the undersigned at the telephone number listed below.

Dated: **August 17, 2005**

Respectfully submitted,
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